IN THE CLAIMS

Claims 1-31 (Canceled)

32. (Currently amended) A nonvolatile memory comprising:

a plurality of nonvolatile memory cells;

a controller;

a plurality of latch circuits;

a plurality of bit lines; and

a plurality of word lines, [[;]] ~~and~~

~~a plurality of memory cells,~~

wherein each of said plurality of nonvolatile memory cells has a first terminal and a second terminal,

wherein each of said word lines are coupled ~~couples~~ to said first terminals of corresponding ones of said plurality of nonvolatile memory cells,

wherein each of said bit lines are coupled ~~couples~~ to said second terminals of corresponding ones of said plurality of nonvolatile memory cells in parallel, and ~~couples~~ to a corresponding one of said latch circuits,

wherein each of said plurality of nonvolatile memory cells coupled to one word line ~~include~~ belongs to an arbitrary one of first ones and second ones,

wherein nonvolatile memory cells belonging to said first ones have already stored first data therein, and each of said nonvolatile memory cells belonging to said first ones has one of a first state and a second state according to said first data,

wherein ~~all of~~ each of nonvolatile memory cells belonging to said second ones have said first state, and

wherein prior to a program operation of said first ones and said second ones, first latch circuits coupled to said first ones via first bit lines and second latch circuits coupled to said second ones via second bit lines are set with first data and second data, respectively, and

wherein ~~in a programming, said controller controls selecting one of word lines, setting said first data to said latch circuits coupled to said first ones via said bit line, setting second data to said latch circuits coupled to said second ones and, supplying a program voltage to said selected word line for storing second data to said second ones coupled to said selected word line and for remaining said first ones stored said first data~~ after setting of the first and second

latch circuits with said first and said second data, said program operation of said first and said second ones are programmed in parallel bit by bit in response to said first data and said second data set in said first and second latch circuits.

33. (Currently amended) A nonvolatile memory according to claim 32,

wherein after said ~~programming~~ program operation, each of said first ones has one of said first state and said second state according to said first data, and each of said second ones has one of said first state and said second state according to said second data.

34. (Currently amended) A nonvolatile memory according to claim 33,

wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a first threshold voltage range and a second threshold range, said first threshold voltage range ~~corresponding~~ corresponds to said first state and said second threshold voltage range ~~corresponding~~ corresponds to said second state, and

wherein said ~~programming moves the threshold~~ program operation is to move a threshold voltage of said second ones coupled to said selected word line to one of said first threshold voltage range and said second threshold voltage range according to said second data.

35. (Previously Presented) A nonvolatile memory according to claim 34,

wherein ~~a~~ higher limit voltage of said first threshold voltage range is lower than a lower limit voltage of said second threshold voltage range.

36. (Currently amended) A nonvolatile memory according to claim 35,

wherein said first threshold voltage range ~~corresponds to~~ indicates an erase state and said second threshold voltage range ~~corresponds to~~ indicates a program state.

37. (Currently amended) A nonvolatile memory comprising:

a plurality of nonvolatile memory cells;

a controller;

a plurality of bit lines;

a plurality of word lines; and

~~a plurality of nonvolatile memory cells,~~

a latch unit,

wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges, ~~including~~ a first threshold voltage range of said plurality of threshold voltage ranges ~~corresponding to~~ indicates an erase state and a second threshold voltage range of said plurality of threshold voltage ranges ~~corresponding to a~~ indicates a program state, and has a first terminal, a second terminal and a well region,

wherein each of said word lines couples to said first terminals of corresponding ones of said nonvolatile memory cells,

wherein each of said bit lines couples to said second terminals of corresponding ones of said nonvolatile memory cells in parallel,

wherein each of said nonvolatile memory cells coupled to one word line ~~include~~ belongs to an arbitrary one of first ones and second ones,

wherein each of said threshold voltages of nonvolatile memory cells belonging to said first ones ~~are~~ is

within either said first threshold voltage range or said second threshold voltage range according to stored first data,

wherein ~~all~~ each of said threshold voltages of nonvolatile memory cells belonging to said second ones ~~are~~ is within said first threshold voltage range,

wherein said well regions of adjacent nonvolatile memory cells coupled to one word line are connected ~~together~~, ~~and~~

wherein said controller ~~controls,~~ carries out a program operation, in response to receiving a first command with a second data, ~~selection of one word line, and supplying of a first voltage to said selected word line for changing the threshold voltage of said second ones from said first threshold voltage range to either said first threshold voltage range or said second threshold voltage range according to said second data, and for remaining the threshold voltage of said first ones remaining in either said first threshold voltage range or said second threshold voltage range according to said first data.~~

wherein in said program operation, said controller selects one word line, reads out first data from first ones coupled to selected word line, and sets said first data and said second data to said latch unit,

wherein after setting said first data and said second data to said latch unit in said program operation, said controller carries out supply of a first voltage to said selected word line so that said first ones and second ones are programmed in parallel in response to said first data and said second data set in said latch unit.

38. (Currently amended) A nonvolatile memory according to claim 37,

wherein said controller controls, in response to receiving a second command, selection of one word line and supplying of a second voltage to ~~said~~ a selected word line for changing each threshold voltage of said first ones and second ones to be within said first threshold voltage range.

39. (Currently amended) A nonvolatile memory according to claim 38, ~~further comprising~~ wherein said latch unit comprises a plurality of latch circuits,

wherein each of said latch circuits couples to a corresponding bit line,

wherein said controller controls setting of a flag to said latch circuits coupled to memory cells objected to change threshold voltage from said first threshold voltage

range to said second threshold voltage range before supplying said first voltage to said selected word line.

40. (Currently amended) A nonvolatile memory according to claim 39,

wherein said controller controls changing of threshold voltages of memory cells, ~~said~~ threshold voltages of ~~being~~ which are within said second threshold voltage range, to within an intermediate range between said first threshold voltage range and said second threshold voltage range before supplying said first voltage to said selected word line.